WHAT IS CLAIMED IS:

1. A method of forming a semiconductor device comprising:

forming a structure on a wafer, the structure having a first layer and a mask layer, the first layer having a layer formed of pre-doped polysilicon and;

oxidizing the wafer creating an oxidized layer prior to removing the mask layer; and

removing the oxidized layer.

2. The method of claim 1 wherein the first layer is about 1500 Å to about 2500 Å in thickness.

3. The method of claim 1 wherein the first layer is about 1800 Å in thickness.

4. The method of claim 1 wherein the pre-doped polysilicon is pre-doped with a material selected from the group consisting essentially of phosphorous, nitrogen, arsenic, and antimony.

5. The method of claim 1 wherein the structure is a gate structure and includes an insulator layer.

6. The method of claim 5 wherein the insulator layer is formed of a material selected from the group consisting essentially of oxide, silicon dioxide, and combinations thereof.

7. The method of claim 1 wherein oxidizing is performed by rapid thermal oxidation (RTO).

8. The method of claim 7 wherein RTO is performed at a temperature about 900° C to about 1010° C.

9. The method of claim 7 wherein RTO is performed for about 5 seconds to about 15 seconds.

10. The method of claim 1 wherein removing the mask layer is performed by a wet dip in phosphoric acid.

11. The method of claim 1 wherein the mask layer includes a plasma-enhanced oxygen (PEOX) layer and a silicon oxynitride (SiON) layer.

12. The method of claim 11 wherein the PEOX layer is about 200 Å to about 300 Å in thickness.

13. The method of claim 11 wherein the PEOX layer is about 260 Å in thickness.

14. The method of claim 11 wherein the SiON layer is about 100 Å to about 200 Å in thickness.

15. The method of claim 11 wherein the SiON layer is about 150 Å in thickness.

16. A method of forming a semiconductor device on a wafer having a substrate comprising:

forming a polysilicon layer on the substrate;

pre-doping the polysilicon layer;

forming a mask layer on the polysilicon layer;

etching the mask layer, the polysilicon layer, and the gate oxide;

oxidizing the wafer creating an oxidized layer; and

removing the mask layer and the oxidized layer.

17. The method of claim 16 wherein pre-doping is performed with a material selected from the group consisting essentially of phosphorous, nitrogen, arsenic, and antimony.

18. The method of claim 16 wherein the polysilicon layer formed on an insulator layer is formed of a material selected from the group consisting essentially of oxide, silicon dioxide, and combinations thereof.

19. The method of claim 16 wherein oxidizing is performed by rapid thermal oxidation (RTO).

20. The method of claim 19 wherein RTO is performed at a temperature about 900° C to about 1010° C.

21. The method of claim 19 wherein RTO is performed for about 5 seconds to about 15 seconds.

22. The method of claim 16 wherein removing the mask layer is performed by a wet dip in phosphoric acid.

23. The method of claim 16 wherein the polysilicon layer is about 1500 Å to about 2500 Å in thickness.

24. The method of claim 16 wherein the polysilicon layer about 1800 Å in thickness.

25. The method of claim 16 wherein the mask layer includes a plasma-enhanced oxygen (PEOX) layer and a silicon oxynitride (SiON) layer.

26. The method of claim 25 wherein the PEOX layer is about 200 Å to about 300 Å in thickness.

27. The method of claim 25 wherein the PEOX layer is about 260 Å in thickness.

28. The method of claim 25 wherein the SiON layer is about 100 Å to about 200 Å in thickness.

29. The method of claim 25 wherein the SiON layer is about 150 Å in thickness.